

### REMARKS

Claims 10-15 are pending in the application. Claims 10 and 13 have been amended, Claims 16 and 17 have been added, leaving Claims 10-17 for consideration upon entry of the present amendment.

Support for the new Claims 16-17 and the amendments to Claims 10 and 13 can at least be found in Figures 3 and 4E and in the corresponding discussion in the specification.

No new matter has been introduced by these amendments. Reconsideration and allowance of the claims are respectfully requested in view of the above amendments and the following remarks.

#### Claim Rejections Under 35 U.S.C. § 103(a)

Claims 10-12 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Kunii (U.S. 5,412,493) in view of Tanabe et al. (U.S. PG-Pub 2002/0072158).

Claims 13-15 are rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Kunii in view of Tanabe.

For an obviousness rejection to be proper, the Examiner must meet the burden of establishing that all elements of the invention are disclosed in the prior art; and that the prior art relied upon, coupled with knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated the skilled artisan to modify a reference or combined references. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988); *In Re Wilson*, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970); *Amgen v. Chugai Pharmaceuticals Co.*, 927 U.S.P.Q.2d 1016, 1023 (Fed. Cir. 1996).

Claims 10-15 comprise, *inter alia*, the following limitations: "said first gate insulating film covers said semiconductor film...said second gate insulating film is integrally formed over said first gate insulating film, which covers said semiconductor film; said second gate insulating film has a smaller film thickness in a region not covered with said gate electrode than that in said region covered with said gate electrode; and said second gate insulating film covers said first gate insulating film in said region not covered with said gate electrode in which said second gate insulating film has said smaller film thickness."

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In making the rejection, the Examiner states that Tanabe discloses "a silicon nitride insulating film 6, with a smaller film thickness in a region not covered with a gate electrode 7 than a silicon nitride insulating film in a region covered with said gate electrode." However, although Tanabe discloses that a portion of the first gate insulating film formed on the semiconductor film is removed above the semiconductor film, Tanabe fails to disclose providing a suggestion to reduce the film thickness of the second gate insulating film formed on the first gate insulating film formed on the semiconductor film in a region not covered with the gate electrode. In addition, the thin portion of the silicon nitride insulating film 6 pointed out by the Examiner has a thinner total thickness of the insulating films by an amount corresponding to the thickness of the first gate insulating film, because the first gate insulating film formed below is removed.

In Applicant's claimed invention, the first gate insulating film covers the semiconductor film and the second gate insulating film is formed covering the first gate insulating film. Thus, even when a silicon oxide is employed as the first gate insulating film and a second gate insulating film as defined in, for example, Claim 11 of the present disclosure or even when a polycrystalline silicon film is employed as the semiconductor film as defined in Claim 12, the semiconductor film is covered with the first gate insulating film, and it is possible to prevent direct exposure of the semiconductor film to an etching solution or generation of deficiency in the semiconductor film due to distortion in the interface. Because the first gate insulating film is further covered with the first gate insulating film, it is possible to prevent intrusion of impurities into the semiconductor film from the outside by employing, for example, a silicon nitride film which is dense as the second gate insulating film. In addition, by reducing the thickness of the second gate insulating film in a region not covered with the gate electrode, the energy required for doping impurities into the semiconductor film using the gate electrode as a mask can be reduced.

In Tanabe, the second gate insulating film covers the semiconductor film in a region in which the first gate insulating film is removed above the semiconductor film, and therefore, the above-described advantages of the presently claimed invention cannot be obtained. Further, Tanabe fails to even suggest the necessity for obtaining such advantages.

In Kunii, the second gate insulating film is completely removed above the semiconductor film in a portion of the second gate insulating film not covered with the gate electrode and does not

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suggest reducing the thickness of the second gate insulating film in a region not covered with the gate electrode.

Thus, in Tanabe and Kunii, one of the two gate insulating films is completely removed in the region in which the total thickness of the gate insulating film is reduced. Thus, even when these citations are combined, only a structure having one of the insulating films completely removed can be obtained, and therefore, the combination of these citations will not motivate a person with ordinary skill in the art to make the presently claimed invention. Therefore, the present invention cannot be viewed as obvious from these citations. Accordingly, Claims 10-15 are allowable.

Claims 10-12 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Ogawa (JP 5-335578) in view of Tanabe.

Claims 13-15 are further rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Ogawa in view of Tanabe.

See above for the teachings of Tanabe.

With regards to Ogawa, Ogawa fails to even suggest the necessity for partially changing the thickness of the gate insulating film. Therefore, Ogawa cannot be combined with Tanabe in which the first gate insulating film is removed above the semiconductor film, and even when these citations are combined, it is possible to only obtain the structure of Tanabe. As such, the combined references fail to teach or suggest at least one claimed element. Since the combined references fail to teach or suggest at least one claimed element, Claims 10-15 are non-obvious and therefore are allowable.

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In view of the foregoing, it is respectfully submitted that the instant application is in condition for allowance. Accordingly, it is respectfully requested that this application be allowed and a Notice of Allowance issued. If the Examiner believes that a telephone conference with Applicant's attorneys would be advantageous to the disposition of this case, the Examiner is cordially requested to telephone the undersigned. In the event the Commissioner of Patents and Trademarks deems additional fees to be due in connection with this application, Applicant's attorney hereby authorizes that such fee be charged to Deposit Account No. 06-1130.

Respectfully submitted,

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